High performance organic nonvolatile memory transistors based on HfO_2 and poly(α-methylstyrene) electret hybrid charge-trapping layers

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In this work, we fabricated a high performance flash-type organic nonvolatile memory transistor, which adopted polymer-electret poly(α-methylstyrene) (PαMS) and HfO_2 films as hybrid charge trapping layer (CTL). Compared with a single HfO_2 or PαMS CTL structure, the hybrid HfO_2/PαMS CTL structure can provide enhanced charge trapping efficiency to increase the device operation speed and reduce the leakage current to boost the device reliability. The fabricated nonvolatile organic memory transistors with the hybrid CTL shows excellent electrical properties, including low operation voltage (8 V), high speed (<10 ms), excellent data retention (on-off current ratio of 2.6×10^4 after 10^4 s), and good endurance (more than 2000 program/erase cycles). The present work provides useful idea for the design of future low-power consumption and highly reliable organic nonvolatile memories. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4997748]

A flash-type organic memory transistor based on an organic thin film transistor (OTFT) is one of the important organic nonvolatile memory devices.[1–12] In recent years, it has been intensively investigated by different groups,[2,4–7,9–15] in which a thick SiO_2 film is often used as the blocking oxide and polymer-electret or metal nanoparticles are often used for charge trapping. Consequently, the memory devices always exhibit high operation voltage (usually larger than 20 V) and low program/erase (P/E) speed (often longer than 1 s).[5–12] To reduce the operation voltage and increase the operation speed, high permittivity (high-*k*) materials have been adopted into the flash-type memory devices as blocking oxide or even as charge trapping materials.[1–4] For example, Yeh *et al.*[3] reported a low-operation-voltage (<20 V) memory devices through high-*k* HfO_2 blocking oxide and polymer electret layer. However, the trapped charges start to degrade seriously after only 10^3 s. Nam *et al.*[1] reported a memory device with very low operation voltage (5 V), in which high-*k* polymer poly(vinyl alcohol) was used as both blocking oxide and charge trapping layer (CTL). Unfortunately, the reported P/E pulse width was as long as 3 s. Jeong *et al.*[4] reported the poly(3,5-benzoic acid hexafluoroisopropylidenediphthalimide)-OTFT memory device by using a 50 nm Al_2O_3 film as blocking oxide, and the device shows a low operation voltage down to 10 V and comparatively good charge retention ability (>10^4 s). The disadvantage of this device is that the writing operation requires the assistance of light illumination, which means that one more process is needed for its high performance operation. Summarized from the reported results, the introduction of high-*k* materials into an organic flash memory transistor can improve their electrical performance in some aspects. However, their overall performances such as operation voltage, operation speed, and reliability still have a long distance to meet the requirements for future commercial applications. Therefore, it is still very necessary to explore different materials or device structures to further enhance their overall electrical performances.

In our earlier study,[16] the electron-beam evaporated HfO_2 film shows an excellent charge trapping ability and long-term charge retention. In another recent work by Zhuang *et al.*,[17] insulating HfO_2 dielectric film was adopted to be the CTL in the organic flash memory, and a large memory window and long data retention have been achieved. However, the reported program/erase voltage in their HfO_2-flash memory transistor is 60 V for 5 s, which is too high for real applications. The reason may be due to the thick SiO_2 blocking layer used in the device. Polymer-electret poly(α-methylstyrene) (PαMS) usually has a nonpolar and hydrophobic surface,[8] and it has been widely used as a surface modification layer to reduce the surface energy of the dielectric film below.[18] PαMS has also been reported to be a polymer electret material, which can be used for charge trapping for memory applications.[8] Considering the unique properties of PαMS and an excellent charge trapping ability of the HfO_2 film, in this work, we proposed a flash-type organic memory transistor with the hybrid charge trapping layer of HfO_2/PαMS. The present organic memory device based on inorganic high-*k*/polymer electret hybrid

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charge trapping layers shows significantly enhanced memory properties in terms of low operation voltage, high P/E speed, and high reliability. Our work will provide useful idea to design high performance organic nonvolatile memory devices.

The as-proposed flash memory transistor was constructed using an OTFT structure with a bottom gate/top contact configuration. Figure 1(a) is a schematic diagram of the cross-sectional OTFT memory device. A heavily doped $P^{++}Si$ (100) substrate was utilized as a bottom gate. The wafer was first cleaned by wet chemical solution and then was dipped in diluted hydrofluoric acid (HF, 1%) to remove the surface oxide. Then, a ~20 nm thick Al_2O_3 layer was fabricated by the atomic layer deposition (ALD) technique with the precursor of trimethylaluminum [Al $(CH_3)_3$, TMA] at a substrate temperature of 250 °C. One layer of ~6 nm HfO_2 film was deposited onto the Al_2O_3 layer by electron-beam evaporation at a substrate temperature of 250 °C. After the completion of the deposition process, the dielectric layers were annealed at 300 °C in an O_2 atmosphere for 30 min. Subsequently, one poly(a-methylstyrene) (PαMS) layer with ~10 nm thickness was spin-coated on the top of the HfO_2 film. The spin-coated PαMS film was annealed in air at 120 °C for 5 min to finish the fabrication of the HfO_2/PαMS hybrid charge-trapping layer. Thereafter, a 40 nm pentacene film was deposited onto the PαMS surface by thermal evaporation at a rate of 0.02 nm/s and a substrate temperature of 50 °C. Finally, the source/drain electrodes were fabricated by depositing a 40 nm-thick Cu film using thermal evaporation with a shadow mask. The resulting semiconductor channel length and width were 50 μm and 750 μm, respectively. The electrical properties of the OTFT memory devices were measured by a high-precision semiconductor analyzer (Agilent B1500A) on a Janis high-vacuum probe station at room temperature. The high-resolution transmission electron microscopy (HRTEM, JEOL2100F) was used to examine the cross-sectional microstructures of the organic memory transistor. The electronic structures of the Al_2O_3/HfO_2/PαMS dielectric stack were investigated by X-ray photoelectron spectroscopy (XPS) and an ultraviolet photoelectron spectrometer (UPS) (ESCALAB 250 Xi).

The cross-sectional structure of the actual memory transistor is shown in Fig. 1(b), where the HRTEM image of the $P^{++}Si$-Al_2O_3-HfO_2-PαMS-pentacene structure is presented. Here, the Al_2O_3 layer and HfO_2 layer were 20 nm and 6 nm in thickness, respectively. The high-k Al_2O_3 and HfO_2 films were both fully amorphous. Due to the relatively low processing temperature (300 °C), a clear interface between the bottom Si gate and the Al_2O_3 layer can be identified without undesirable interfacial SiO_2. As the organic PαMS and pentacene layers could not be distinguished from each other in the HRTEM imaging, only the total thickness of ~50 nm for the two layers was identified. To characterize the memory properties of the OTFT devices, the drain current-gate voltage (I_{ds}-V_{gs}) curves at different forward-backward voltage scanning cycles were measured, as shown in Fig. 1(c). The sweeping gate voltages varied from ±9 V to ±14 V, with V_{ds} = −3.0 V. The transfer curves exhibit the anticlockwise memory hysteresis loops during the positive-negative-positive voltage scanning cycles, suggesting a typical charge-trapping effect on the hybrid CTL memory transistors. For the scanning voltages of ±9 V and below, no memory effect was observed. Relatively small memory window was measured as the scanning gate voltages (±11 V). With further increasing the scanning voltages, a large memory window of ~4.8 V was observed under ± 14 V sweeping voltages, indicating significant charge trapping effects on the hybrid dielectric stacks.

For comparison, the organic memory transistors with a single HfO_2 or single PαMS CTL were also fabricated and characterized; the corresponding device structure and measurement results are shown in Figs. S1 and S2, respectively. Only very weak memory effect can be observed for the HfO_2-only CTL memory device under 5 V or smaller

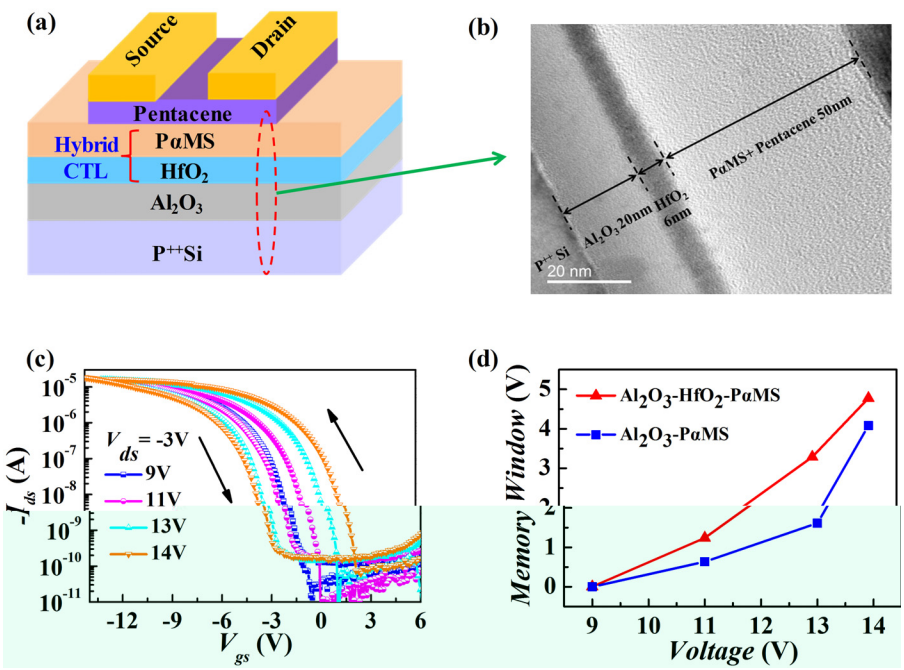

FIG. 1. (a) A schematic diagram of the OTFT memory device; (b) the cross-sectional HRTEM image of the $P^{++}Si$/Al_2O_3/HfO_2/PαMS/pentacene stacked structure; (c) the drain current-gate voltage hysteresis characteristics of the OTFT memory devices with HfO_2/PαMS hybrid charge-trapping layers; and (d) dependence of memory window width on the sweeping gate voltages for the hybrid structure device and PαMS-only device.

sweeping voltages, as shown in Fig. S1(c). When further increasing the sweeping gate voltage to 7 V, the device starts to become very leaky and no reliable memory effect is available. The gate leakage current will increase to 10^{-2} A under −7 V bias voltage, as shown in Fig. S1(d). For the PαMS-only CTL memory devices, a clear memory effect can be observed when the scanning voltage increases to 12 V, as shown in Fig. S2(c). However, the memory window of PαMS-only devices is still smaller than that of the HfO_2/PαMS hybrid CTL devices, as shown in Fig. 1(d). The present results demonstrate that the hybrid CTL is more efficient to capture charges than that of the HfO_2 or PαMS single CTL. From Figs. S1 and S2, we can also learn that the grain size of the pentacene film grown on the HfO_2 surface is much smaller than that grown on the PαMS-surface. Correspondingly, the saturation drain current of the HfO_2-only device is also much smaller than that of the PαMS-only device. The PαMS layer plays a very important role not only for charge trapping but also for surface modification to improve the interface quality between the dielectric layer and the organic semiconductor.

The memory characteristics of the hybrid CTL devices were further investigated by examining the drain current response to the P/E pulses with different heights and widths. After P/E processes, the drain current was recorded at a gate voltage of −2 V and a constant drain voltage of −3 V. Figures 2(a) and 2(b) depict the ON/OFF drain currents responding to different P/E pulses. At fixed pulse heights of 8 V, the ON/OFF drain currents were measured at different pulse widths ranging from 10^{-6} s to 2×10^{-2} s [Fig. 2(a)]. Nearly, no separation of ON/OFF drain currents could be observed at the pulse width of 10^{-3} s or smaller. The separation of ON/OFF current appeared at pulse widths larger than 1 ms, where an ON/OFF ratio of 3.5×10^4 was observed for a 5 ms pulse width. Figure 2(b) displays the variation of ON/OFF drain current as a function of the pulse height from 4 V to 8 V with a 10 ms pulse width. A 7 V pulse amplitude could switch the ON/OFF drain current ratio to more than 10^4, which implied that the present hybrid CTL memory device had much smaller operation voltage and higher working speed when comparing with most of the organic memory transistors. For example, Chou *et al.*[5] fabricated polymer-electret OTFT memory devices with different thiophene chain lengths requiring 100 V and 1 s operation pulse. Cross-linked core-shell nanoparticle based memory devices also required 50 V working voltage as reported by Chen's group.[6] By using donor-acceptor poly(3-hexylthiophene)-block-pendent poly(isoindigo), Lo *et al.*[7] prepared a memory device without an additional charge storage layer with an operation voltage of 100 V.

The reliability of PαMS/HfO_2 hybrid trapping layer based OTFT memory devices was also examined. Figure 3(a) shows the ON/OFF drain currents changes as a function of repetitive cycles of P/E pulses, where magnitude and width of the pulses were set to be 8 V and 10 ms, respectively. Only a small degradation was obtained after 2000 P/E cycles, and the ON/OFF ratio of drain current remains at 4.1×10^3. This indicates the good endurance of the devices. When comparing with most of the reported electret-type OTFT memories that exhibited significant degradation after only several hundreds of P/E cycles,[9–12] the present memory device exhibits much-improved endurance characteristics. Figure 3(b) illustrates the drain current retention characteristics after a 8 V/10 ms programming pulse or −8 V/10 ms erasing pulse. The ON/OFF drain current was recorded at fixed voltages V_{gs} of −2 V and V_{ds} of −3 V. The OTFT memory devices showed excellent charge retention, where the ON/OFF current ratio retained 2.6×10^4 even after 10^4 s. Furthermore, by extending the retention time to 10 years by extrapolation, the ON-OFF current ratio still can remain at 4.2×10^3. We made a comparison of the overall electrical performances between the present device and other reported results for organic nonvolatile memories, as shown in the supplementary material Fig. S3. The comprehensive electrical performance of our memory devices is much better than those of most of the reported polymer-electret based OTFT memory devices, indicating the advantages of the hybrid charge trapping structure for high performance nonvolatile organic memory applications.

The excellent electrical performances of the present hybrid CTL memory transistors could be attributed to the following mechanisms. The low voltage and high-speed operation is attributed to the unique structure of the hybrid CTL. Both HfO_2[17] and PαMS[8] have excellent charge trapping ability; therefore, the hybrid charge trapping layer can enhance the charge trapping efficiency of memory devices. From Fig. 1(d), we can clearly learn that the hybrid CTL device has a larger memory window than that of the PαMS-only device. The enhanced charge trapping efficiency will be effective to reduce the P/E pulse amplitude and width. For the PαMS-only device, a long programming pulse width of

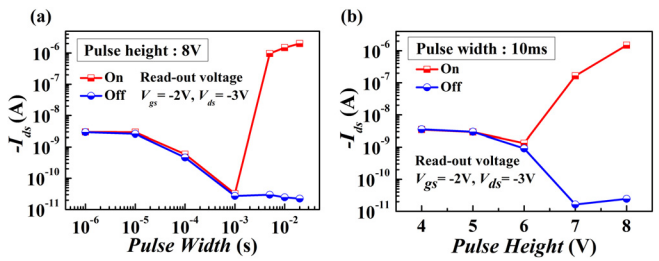

FIG. 2. (a) Dependence of drain current on the P/E pulses with different widths. The pulse height is fixed to be 8 V; (b) dependence of drain current on the P/E pulses with different magnitudes. The pulse width is fixed to be 10 ms. All of the drain current values are read out at V_{gs} of −2 V and V_{ds} of −3 V.

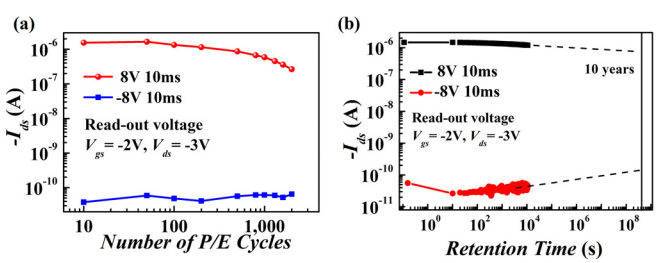

FIG. 3. (a) Endurance property of the OTFT memory devices for repeated P/E pulses of 8/−8 V 10 ms; (b) drain current retention characteristics of the memory devices. The drain current are monitored with time after programing pulse (8 V, 10 ms) and erasing pulse (−8 V, 10 ms) at a read-out V_{gs} of −2 V and V_{ds} of −3 V.

1 s is needed to obtain a high ON/OFF ratio during the retention measurement, as shown in Fig. S4(a), while only 10 ms pulse width is needed for the hybrid CTL device, as shown in Fig. 3(b). The high dielectric constant of HfO_2 will keep the effective P/E electric field not much degraded even though the total physical thickness of charge trapping layer is increased, which is also beneficial to the low voltage operation of the device.[19,20]

The high insulating property or low leakage current of the hybrid dielectric stack will be the very important reasons for the excellent reliability of the memory devices. The hybrid charge trapping layer structure has been studied by Gao and Chou *et al.*[2,21] In their work, they used conductive nanoparticles and polyamide or graphene oxide as the CTL. Although an additional nanoparticle layer may improve the trapping efficiency of the memory device, it is believed that high leakage current will be one of the principal drawbacks to limit its use in flash type organic memories. In this work, both of the charge trapping layers are insulating films, which will be very beneficial to provide a low leakage current in the gate dielectric stack. To confirm this assumption, we also monitored the gate leakage current during the drain current retention measurement. As shown in Fig. S4(b), the leakage current biased at a read voltage of −2 V is below 3×10^{-11} A during the whole measurement time. While for PαMS-only memory transistor, the gate leakage current biased at a reading gate voltage of −3 V is between 10^{-9} A and 10^{-7} A, as shown in Fig. S4(c). Correspondingly, a worse retention property of drain current is observed, which implies that the insulating property plays a significant role on the data retention of the present memory devices.

Another important reason for the excellent retention is strong confinement for the trapped charges during retention, which is provided by the deep defect levels of HfO_2[16] as well as high potential barrier between PαMS and HfO_2. To confirm this assumption, the electronic structures of the inorganic high-*k*/polymer-electret dielectric stack were investigated by using XPS and UPS.[22–24] The detailed results are shown in Fig. S5. The band alignment of the Al_2O_3/HfO_2/PαMS dielectric stack can be determined, which was shown in Fig. 4(a). The band gaps of Al_2O_3, HfO_2, and PαMS were determined to be 7.4 eV, 5.1 eV, and 6.7 eV, respectively. A large ΔE_c of 1.26 eV has been observed between HfO_2 and PαMS, which will provide a strong electron confinement during charge retention. Based on the above XPS and UPS experimental results, we proposed a carrier transportation model during P/E processes of the hybrid CTL memory transistors. For a short positive program pulse (<1 ms), no electrons would be trapped in PαMS since the pentacene channel was of p-type. By contrast, the holes in pentacene will be depleted further away from the interface of pentacene/insulator, leading to declined drain current [Fig. 2(a)]. This carrier transport behavior under short pulse (<1 ms) could be the reason why the ON currents decreased as the program pulse width increased. At a relatively large programming voltage pulse (>1 ms in this case), the electrons injected from source/drain electrodes starts to be trapped in the PαMS layer [process "a" in Fig. 4(b)]. Further increase in scanning voltage or pulse width will supply the electrons with high enough energy to overcome the potential barrier between pentacene and PαMS, and hence the charges became trapped by the defect levels in hafnium oxide [process b in Fig. 4(b)]. Therefore, an enhanced memory effect can be observed for devices with the HfO_2/PαMS hybrid charge trapping layer when compared to devices with only single PαMS layer. The charge transport behavior during the erasing process is opposite to that in the programming process. Upon the application of a negative pulse, the holes will be injected into the organic-inorganic hybrid charge-trapping layer [processes c and d in Fig. 4(b)]. Meanwhile, the previously stored electrons would tunnel out (process e) or recombine with the newly injected holes (process f).

Low operation voltage and highly reliable organic nonvolatile memory devices have been prepared using high-*k* HfO_2 and polymer-electret PαMS as the hybrid CTL. The P/E voltages can reach 8/−8 V and operation speed up to 10 ms. Furthermore, the ON/OFF ratio of drain current can remain at 2.6×10^4 after 10^4 s retention and at 4.1×10^3 after

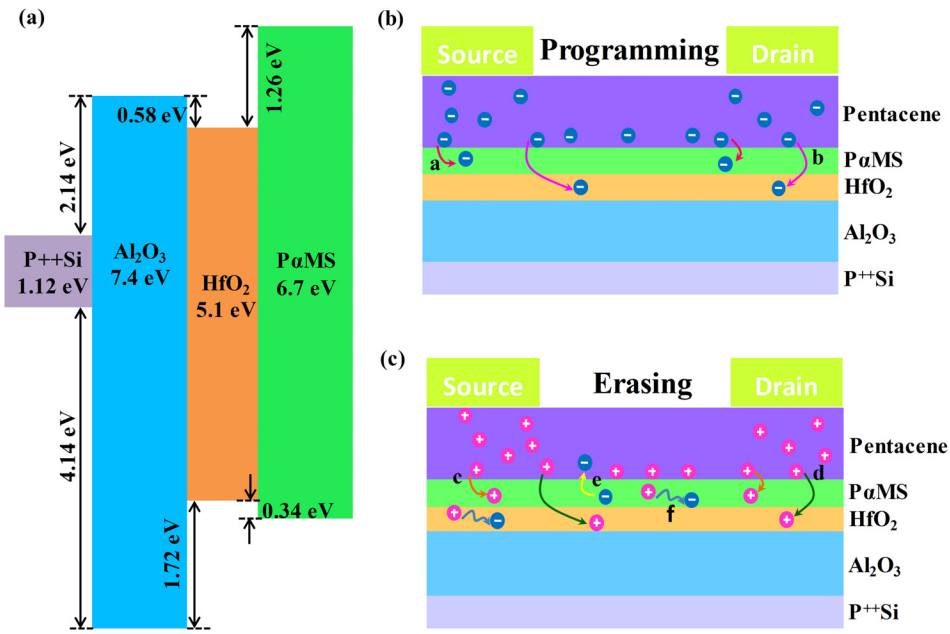

FIG. 4. (a) Band alignments of the Al_2O_3/HfO_2/PαMS dielectric structure from the XPS and UPS results; (b) a schematic diagram of charge transport in the memory device during the programming process; and (c) a schematic diagram of charge transport in the memory device during the erasing process.

2000 P/E endurance cycles, indicating the highly reliable operation of the devices. The excellent electrical performances of the present hybrid CTL memory transistors are attributed to the enhanced charge trapping efficiency, reduced gate leakage current, and strong charge confinement in the hybrid CTL structure, which indicates its great potential for applications in the future high-performance organic memory devices.

See supplementary material for details of the pentacene atomic force microscopy measurement results, electrical properties of HfO_2-only and PαMS-only CTL memory transistors, a comparison of the overall electrical performance of the hybrid CTL memory transistor with that of the other flash-type OTFT memory devices, and the XPS and UPS results of the Al_2O_3/HfO_2/PαMS dielectric stack.

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